A STUDY ON HARMONICS INVESTIGATION OF A HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR FIVE LEVEL INVERTER WITH SVPWM AND SPWM

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ABSTRACT: This research paper gives the idea about the harmonics investigation of a hybrid active neutral point clamped flying capacitor five level inverter with svpwm and spwm. In the field of high power and medium voltage application, the multilevel inverters seem to be the most promising alternative. The five-level hybrid topology combining features of neutral point clamped and flying capacitor Multi-level inverters is shown here. The topology provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connection of semiconductor devices, keep the balanced operation of dc-link capacitors while keeping the number of costly components such as capacitors and switches low.

KEYWORDS: Neutral Point flying Clamped Inverter (NPFCI), Total Harmonic Distortion (THD), Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM).

I. INTRODUCTION

With Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly [1] As a result; a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors The inverters in such application areas as stated above should be able to handle high voltage and large power.

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and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages.

However, the series connection of switching power devices has big problems [13], namely, non-equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

Multilevel converters are a very attractive solution for medium-voltage high-power conversion applications; such as motor drives, microgrids, and distributed generation systems.

The main features of these topologies, as compared with the two-level voltage-source converters (VSC), are their capabilities to reduce:

1) Harmonic distortion of the ac-side waveforms;
2) dv/dt switching stresses;
3) Switching losses; and

Multilevel inverters have gained interest during the last three decades due to the increasing demand for medium to high voltage converters for a variety of high power applications. Different topologies have been proposed to fit the requirements of different applications.

For medium voltage inverters, cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) are the primary topologies. Among them, NPC and FC provide a common dc-link which is a strict requirement for many applications [6].

FC inverter uses capacitors to generate output voltage levels. The availability of interphase l redundant states in this topology can provide both capacitor voltage balancing and power loss distribution among switches [7]. However, increased numbers of flying capacitors at higher levels that increases the initial cost and maintenance surcharges and decreases the reliability of the inverter along with the capacitor pre-charge in some applications are the main drawbacks of this topology [8].

NPC inverter uses diodes to clamp the voltage levels generated at the dc-link capacitors to the output. Excessive number of diodes, unbalanced operation of dc-link's voltage divider capacitors, and uneven distribution of loss among switches are major problems of this topology. Space vector algorithms are available to alleviate the unbalanced loss and capacitor voltage problems based on the inverter's operating condition [5]. Active NPC (ANPC) improves the loss distribution of NPC by replacing diodes with active switches providing alternative neutral point path [9].

Hybrid topologies are viable solutions where higher number of levels is required. Combining the advantages of CHB, FC, and NPC, hybrid inverters can provide loss and voltage balancing while keeping the number of components low. Examples of hybrid topologies combining FC and NPC can be found in [10]–[12], some of which has already found industrial applications. The 5-level FC-ANPC is an example of hybrid topologies that made its way to the industry. The ACS2000 family of medium voltage drives, commercialized by ABB, uses this topology with both active and passive front end configurations.

The main advantage of this topology is the use of a single flying capacitor to generate the output five levels. Compared to other topologies that provide a common dc-link, FC-ANPC has provided an acceptable tradeoff between the cost, performance, and reliability for 5-level applications. The disadvantages of FC-ANPC are high number of switches, series connection of high voltage switches, and poor loss distribution [13]. The proposes a new 5-level hybrid topology based on FC and NPC inverters. The goal of the proposed topology is to overcome the shortcomings of the traditional FC-ANPC. Thus, comparatively, the proposed topology provides better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches per phase leg.

These advantages come at the cost of an additional capacitor and 6 diodes. Nevertheless, the lifetime of each capacitor is expected to prolong due to the half cycle operation and lower rms current.

Power electronic researchers have place in continuous efforts in developing topologies that retain the inherent edges of construction inverters with lesser range of power switches and different extra options.

With the arrival of latest topologies, a larger stress is additionally placed on to research new switching strategies. This is because of the fact that a particular switching strategy for a given topology can result in improvement of harmonic profile of output waveform as well as reduction in switching and conduction power losses. The three switching methods most discussed in the literature are:

- Carrier-based PWM
- Selective Harmonic Elimination
- Space-vector PWM
- Optimized Harmonic PWM (OHPWM)

II. Neutral Point Clamped Multi- Level Inverter

The most commonly used topology in the multilevel inverter is the diode-clamped inverter, in which the diode is used to clamp the dc voltage, to get output voltage steps. Fig. 1 shows a circuit for a three-and a four-level diode clamped inverter. Diodes D_1 and D_2 gives the main difference between the 2-level inverter and the 3- level inverter. Both devices are connected to half the voltage of the dc bus voltage.

The voltage of the N clamped inverter at steady state across each condenser is generally V_{dc} / n-1. Each active switch is required only to block V, but the clamping equipment has different ratings. The inverter with diode clamps provides multiple voltage levels by connecting the phases to a set of condensers.

The concept can be extended to a variety of different levels according to the original invention by increasing the number of condensers. This topology was first described only in three levels, where two condensers were connected across the dc bus and thereby resulted in one additional level. The other level was neutral to the dc bus so that the inverter of the neutral terminology point clamped (NPC) was introduced.

But the neutral point is not accessible with an equal number of voltage levels, and multi-pointed points (MPC) terms can sometimes be used. The diode-clamped inverter implementation was limited to three levels due to problems of voltage balancing of capacitors. The 3- level inverter is now widely used in industrial applications due to industrial developments over the past couple of years.

NPC type multilevel inverters plays crucial role in the field of power electronics and being widely used in different industrial and commercial applications because it possesses low electromagnetic interference and the effectiveness is considerably high. NPC Multilevel inverters have become more preferred over the years in electric high power application with the confirmation of less disturbances and the possibility to operate at lower switching frequencies than typical two-level inverters.

Diode-clamped topology is proposed by Nabae et al. Figure 1 shows a three level diode-camped inverter, where the DC bus voltage is divided into three levels by two bulk capacitors connected in series. The output voltage has three states: Vdc/2, 0, - Vdc/2. The diodes D_1 and D_2 provide a path for the currents at the voltage increments. Diode-clamped inverters are mostly limited to the original three-level structure due to the capacitor voltage balancing issues.

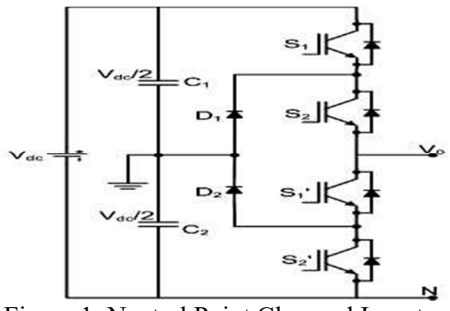

Figure 1: Neutral Point Clamped Inverter

III. Literature Review

This thesis proposes a new 5-level hybrid topology based on FC and NPC inverters. The goal of the proposed topology is to overcome the shortcomings of the traditional FC-ANPC. Thus, comparatively, the proposed topology provides better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches per phase leg.

These advantages come at the cost of an additional capacitor and 6 diodes. Nevertheless, the lifetime of each capacitor is expected to prolong due to the half cycle operation and lower rms current.

The following thesis works have also been referred in completion of this thesis work:

H. Abu-Rub, J. Holtz, and J. Rodriguez, [1] "This paper gives an overview of medium-voltage (MV) multilevel converters with a focus on achieving minimum harmonic distortion and high efficiency at low switching frequency operation. Increasing the power rating by minimizing switching frequency while still maintaining reasonable power quality is an important requirement and a persistent challenge for the industry.

Existing solutions are discussed and analyzed based on their topologies, limitations, and control techniques. As a preferred option for future research and application, an inverter configuration based on three-level building blocks to generate five-level voltage waveforms is suggested. This paper shows that such an inverter may be operated at a very low switching frequency to achieve minimum on-state and dynamic device losses for highly efficient MV drive applications while maintaining low harmonic distortion."

S. Kouro, M. Malinowski, K. Gopal Kumar, J. Paul, L. G. Franquelo, J. Rodriguez, M. A. Pérez, and J. I. Leon,[2] "Multilevel converters have been under research and development for more than three decades and have found successful industrial application. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years.

The aim of this paper is to group and review these recent contributions, in order to establish the current state of the art and trends of the technology, to provide readers with a comprehensive and insightful review of where multilevel converter technology stands and is heading.

This paper first presents a brief overview of well-established multilevel converters strongly oriented to their current state in industrial applications to then center the discussion on the new converters that have made their way into the industry. In addition, new promising topologies are discussed. Recent advances made in modulation and control of multilevel converters is also addressed."

M. Malinowski, K. Gopal Kumar, J. Rodriguez, and M. A. Pérez [3] "Cascaded multilevel inverters synthesize a medium-voltage output based on a series connection of power cells which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy.

Due to these features, the cascaded multilevel inverter has been recognized as an important alternative in the medium-voltage inverter market. This paper presents a survey of different topologies, control strategies and modulation techniques used by these inverters. Regenerative and advanced topologies are also discussed. Applications where the mentioned features play a key role are shown. Finally, future developments are addressed."

J. Rodriguez [4] "Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multi-cell with separate DC sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed.

This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. Special attention is dedicated to the latest and more relevant applications of these converters such as laminators, conveyor belts, and unified power-flow controllers."

J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "Neutral-point-clamped (NPC) inverters are the most widely used topology of multilevel inverters in high-power applications (several megawatts). This paper presents in a very simple way the basic operation and the most used modulation and control techniques developed to date. Special attention is paid to the loss distribution in semiconductors, and an active NPC inverter is presented to overcome this problem.

This paper discusses the main fields of application and presents some technological problems such as capacitor balance and losses. Index Terms—Neutral-point-clamped (NPC) inverters".

J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "This paper presents a technology review of voltage-source-converter topologies for industrial medium-voltage drives. In this highly active area, different converter topologies and circuits have found their application in the market. This paper covers the high-power voltage-source inverter and the most used multilevel-inverter topologies, including the neutral-point-clamped, cascaded H-bridge, and flying-capacitor converters."

B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes[7] "Modulation of flying capacitor and stacked multi cell converters is complicated by the fact that these converters have redundant states that achieve the same phase leg voltage output. Hence, a modulator must use some secondary criteria such as cell voltage balancing to fully define the converter switched state.

Alternatively, the modulator can be adapted to directly specify the cell states, such as has been proposed for the harmonically optimal phase disposition (PD) strategy. However the techniques reported to date can lead to uneven distribution of switching transitions between cells, and the synthesis of narrow switched phase leg pulses.

This paper presents an improved strategy that decouples the tasks of voltage level selection and switching event distribution. Conventional PD and centered space vector pulse width modulation (CSVPWM) strategies are used to define the target voltage level for the converter, and a finite state machine is then used to distribute the transitions to the converter cells in a cyclical fashion."

T. Bruckner, S. Bernet, and H. Guldner, [9] The three-level neutral-point-clamped voltage-source converter (NPC VSC) is widely used in high-power medium voltage applications. The unequal loss distribution among the semiconductors is one major disadvantage of this popular topology.

This paper studies the loss distribution problem of the NPC VSC and proposes the active NPC VSC to overcome this drawback. The switch states and commutations of the converter are analyzed. A loss-balancing scheme is introduced, enabling a substantially increased output power and an improved performance at zero speed, compared to the conventional NPC VSC.

M. Narimani, B. Wu, Z. Cheng, and N. Zargari,[10] In this paper, a new voltage source converter for medium voltage applications is presented which can operate over a wide range of voltages (2.4–7.2 kV) without the need for connecting the power semiconductor in series. The operation of the proposed converter is studied and analyzed. In order to control the proposed converter, a space-vector modulation (SVM) strategy with redundant switching states has been proposed. SVM usually has redundant switching state anyways.

T. B. Soeiro and J. W. Kolar[12] "This paper introduces a novel three-level voltage source converter (VSC) as an alternative to known three-level topologies, including the conventional neutral-point-clamped converter (NPCC), many T-type VSCs, and active NPCC.

It is shown that, operating in the low converter dc-link voltage range, this new solution not only can achieve higher efficiency than many typical three-level structures but also can overcome their drawback of asymmetrical semiconductor loss distribution for some operating conditions."

T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefebvre, "This paper presents a voltage balancing method for stacked multi-cell converters based on phase disposition pulse width modulation.

This method is based on minimizing a cost function to determine the optimum redundant state for capacitor voltage balance for each particular voltage level. The robustness of the proposed voltage balancing method is verified against static and dynamic unbalanced load conditions.

Furthermore, a significant reduction in the switching frequencies of the power devices is achieved by using saw tooth carriers instead of standard triangular carriers without affecting the voltage balancing capability."

R. Naderi and A. Rahmati, [16] "Phase-shifted carrier (PSC) pulse width modulation (PWM) in its conventional form is a good solution for single-phase Cascaded inverters as alternative phase opposition disposition (APOD) PWM for single-phase diode clamped inverters. PSC distributes the switching angles of APOD PWM waveform among the legs uniformly and reduces the switching frequency of each leg.

This paper proposes a modified PSC technique based on partly shifted carriers for all disposition types including phase disposition (PD) which is suitable for three-phase cascaded inverters. Simulation results are also included for using carrier-based space-vector PWM (SVPWM)."

IV. *Multilevel Inverter*

With A dc voltage Vdc series connected capacitors constitute the energy tank for converter providing some nodes to which the multilevel converter can be connected .each capacitor to has the same voltage E_m which is given by

$$E_m = \frac{V_{dc}}{m-1} \quad (1)$$

Where, m denotes the number of levels. The level is referred to as the number of nodes to which the inverter can be accessible. An m-level inverter needs (m-1) capacitors. There are several types of multilevel converters.

The types of multilevel converters are: diode-clamped multilevel converters, flying-capacitor (also referred to as capacitor-clamped) multilevel converters, and cascaded H-bridges multilevel converters At this point, it seems appropriate to discuss the difference between the terms "multilevel converter" and "multilevel inverter."

The term "multilevel converter" refers to the converter itself. Furthermore, the connotation of the term is that power can flow in one of two directions. Power can flow from the ac side to the dc side of the multilevel converter. This method of operation is called the rectification mode of operation. Power can also flow from the dc side to the ac side of the multilevel converter.

This method of operation is called the inverting mode of operation. The term "multilevel inverter" refers to using a multilevel converter in the inverting mode of operation. The line voltage consists of a positive phase-leg *a* voltage and a negative phase-leg *b* voltage. Each phase voltage tracks one-half of the sinusoidal waves.

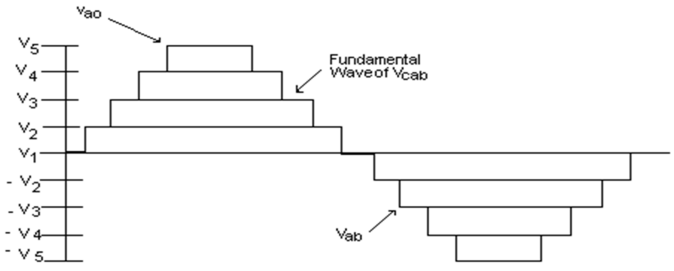

Figure 2: Source Converter

Phase and line voltage waveforms of a 5-level diode-clamp voltage

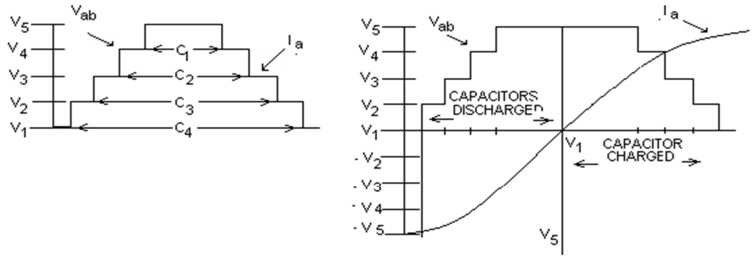

Figure 3: Waveforms Showing Capacitor Charging Profile (a) Voltage and Current in Phase (b) Voltage and Current Are 90^0 Out of Phase.

Multilevel Converter Topologies

The general objective of the multi-level converter is to synthesize a sinusoidal voltage form several levels of voltages by constructing a staircase kind of wave shape. Typically the different voltage levels are obtained from several capacitors connected in series across a DC bus the minimum number of levels of voltage in a multi-level inverter is three.

Basic multi-level topologies have been categorized into the following three types (1) Diode clamped; (2) Flying capacitor; and (3) Cascaded inverter topologies.

PWM Classification

There are many possible PWM techniques proposed in the literature. The classifications of PWM techniques can be given as follows:

1. Sinusoidal PWM
2. Space-Vector PWM
3. Hysteresis band current control PWM

V. Space Vector Pulse Width Modulation (SVPWM)

The space vector pulse width modulation method is an advanced, computation intensive PWM method, which is an excellent feature and is possibly the best among all the PWM techniques for variable frequency drive applications. It has been found wide spread application in recent years, because of its superior performance characteristics.

The space vector pulse width modulation (SVPWM) technique is more popular than conventional technique because of the following excellent features: It achieves the wide linear modulation range associated with PWM, third-harmonic injection automatically.

- It has lower base band harmonics than regular PWM or other sine based modulation methods, or otherwise optimizes harmonics.
- 15% more output voltage than sinusoidal modulation, i.e. better dc-link utilization.
- More efficient use of dc supply voltage.
- Advanced and computation intensive PWM technique.
- Higher efficiency.
- Prevent un-necessary switching, hence less commutation losses.
- A different approach to PWM based on space vector representation of the voltages in the reference frame transformation.

The space vector concept is derived from the rotating field of AC machine which is used for modulating the inverter output voltage. In this modulation technique, the three phase quantities can be transformed to their equivalent two-phase quantity either in synchronously rotating frame (or) stationary frame. From this two-phase component the magnitude of reference vector can be found and is used for modulating the inverter output. The

process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame.

Let the three-phase sinusoidal voltage component be,

$V_a = V_m \sin wt$ (2)

$V_b = V_m \sin(wt - 2\pi/3)$ (3)

$V_C = V_m \sin(wt + 2\pi/3)$ (4)

When this three-phase voltage is applied to the AC machine, it produces a rotating flux in the air gap of the AC machine. This rotating flux component can be represented a single rotating voltage vector. The magnitude and angle of the rotating vector can be found by means of Clark's Transformation as explained below in the stationary reference frame. The representation of rotating vector in Complex plane is shown in Fig.

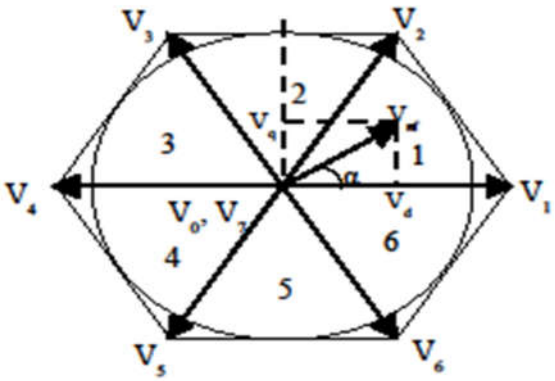

Figure 4: Representation of Rotating Vector in a Complex Plane Space Vector Representation of the Three-Phase Quantity

$|\overline{Vref}| = V_d + jV_Q + 2/3(V_a + aV_b + a^2c)$ (5)

Where a=$e^{j2\pi/3}$

$|\overline{Vref}| = \sqrt{V_d^2 + V_q^2}$; α =$\tan^{-1}\frac{V_d}{V_q}$ (6)

$V_d + jV_q = 2/3\left(V_a + e^{\frac{j2\pi}{3}} V_b + e^{-\frac{j2\pi}{3}} V_C\right)$ (7)

$V_d + jV_q = \frac{2}{3}\left(V_a + \cos\frac{2\pi}{3}V_b + \cos\frac{2\pi}{3}V_c\right) + j\frac{2}{3}\left(\sin\frac{2\pi}{3}V_b + \sin\frac{2\pi}{3}V_c\right)$ (8)

The equation in the matrix form can be written as:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$ (9)

The Space vector PWM treats the sinusoidal voltage as a constant amplitude vector rotating at a constant frequency. This PWM technique approximates the reference voltage V_{ref} by a combination of the eight switching patterns. A three-phase voltage vector is transformed into a vector in the stationary d-q co-ordinate frame. This represents the spatial vector sum of the three-phase voltage.

Conclusion

This research paper gives the idea about the harmonics investigation of a hybrid active neutral point clamped flying capacitor five level inverter with svpwm and spwm. Recent trend in power electronics is based on the use of multilevel inverter technology. Multilevel inverter uses so many switches for generating output. Each switch produces loss in the power. This gives low power at the output. So need for some special topology which have low switch. The CSV PWM technique is more advantageous as compared to SPWM with increased voltage amplitude of 1100V and very less increment of THD.

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